PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ashton et. al.

Serial No.: 10/708,382

Filed: 02/27/2004

Title: LSSD-Compatible Edge-Triggered Shift Register Latch

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Group Art Unit: 2117

Examiner: Guerrier Merant

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P.O. Box 1450
Alexandria, VA 22313-1450

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UNOFFICIAL COMMUNICATION – FOR DISCUSSION PURPOSES ONLY

Examiner Merant:

In furtherance of our telephone conference today, below is 1) a copy of claim 1 as originally filed and 2) a proposed new claim 21 for your approval. The proposed new claim 21 is similar to original claim 1 in that it is directed to a shift register latch that includes circuitry for compensating for delay in a first clock signal that drives the shift register latch. A primary difference of proposed new claim 21 is that the delay is described with a bit more particularity. However, it is Applicants' position that new claim 21 is, for all practical purposes, the same as original claim 1.

Please review both of these claims and let me know if you and your Supervising Patent Examiner (SPE) will accept either or both of these claims in light of our discussion today. As

you and your SPE review these claims, we respectfully ask that you keep in mind, as we discussed during our call today, that Applicants believe original claim 1 is indeed patentable over the cited Gregor et al. patent, as well as the other references of record. Regarding the Gregor et al. patent, Applicants respectfully assert that Gregor et al. are completely silent on providing a shift register latch that compensates for delay on a clock signal used to drive the shift register latch. However, it is precisely this delay-compensation that original claim 1 requires.

1. **(Original)** An integrated circuit, comprising:
   a) at least one shift register latch, comprising:
      i) a first latch;
      ii) a second latch in electrical communication with said first latch;
      iii) an input for receiving a first clock signal; and
      iv) a circuit, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal.

21. (**Proposed New**) An integrated circuit, comprising:
   b) a first shift register latch responsive to a first clock signal;
   c) at least one second shift register latch responsive to the first clock signal, wherein the first clock signal at said at least one second shift register latch has a delay relative to the first clock signal at said first shift register, said at least one second shift register latch comprising:
      i) a first latch;
      ii) a second latch in electrical communication with said first latch;
      iii) an input for receiving the first clock signal; and
      iv) a delay-compensation circuit connected between said input and said first latch, said delay-compensation circuit configured to generate a second clock signal as a function of the first clock signal so as to compensate for the delay in the first clock signal.

Thank you for your time and consideration. I look forward to your comments as we move forward with this application. If you have any questions, or would like to discuss the proposed new claim 21 in more detail, please contact me directly at (802) 846-8305.

Respectfully submitted,

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